

high speed serdes devices pdf

High Speed Serdes Devices and Applications (1/ftx)*m TXxDCLK where: m = 8, 10, 16, or 20 p = 4, 4, 8, or 10 (1/ftx)*p TXxD[19:0] Ts Th Fig. 2.5 Input data interface timing 2.2.2 Transmitter Signal Characteristics Signal level and slew rate requirements vary for the various serial data standards.

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High Speed Serdes Devices and Applications

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A device called Serializer/Deserializer (SerDes) allows data to transfer in a serial manner, and is now playing a more and more important role in modern high speed applications. Such device is capable of converting data from parallel to serial and vice versa, as is illustrated in a simplified model in Figure 2.3.

HIGH SPEED CMOS SERDES DESIGN AND SIMULATION USING CADENCE

Such devices are differentiated from source- Keywords SERDES, Clock and data recovery, High speed synchronous interface in that the receiver device contains a Serdes, Parallel clock SERDES, Embedded clock SERDES, 8b/10b SERDES, Bit interleaving SERDES clock data recovery (CDR) circuit dynamically determines the optimal sampling point of the data signal based upon the transition edges if the signal.

High speed serial link design (SERDES) Introduction

HSS devices are the dominant form of input/output for many (if not most) high-integration chips, moving serial data between chips at speeds up to 10 Gbps and beyond. Chip designers with a background in digital logic design tend to view HSS devices as simply complex digital input/output cells.

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High Speed Serdes Devices and Applications provides a broad understanding of High Speed Serdes (HSS) device usage. The material focuses on HSS devices, and the consolidation of related topics into a single text. Chip and system designers using HSS devices must have detailed knowledge of both the features and functions of the HSS device, and the applications in which they are used.

High Speed Serdes Devices and Applications | David Robert

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1 Intel® MAX® 10 High-Speed LVDS I/O Overview The Intel® MAX 10 device family supports high-speed LVDS protocols through the LVDS I/O banks and the Altera Soft LVDS IP core. The LVDS I/O

banks in Intel MAX 10 devices feature true and emulated LVDS buffers: True LVDS buffers support LVDS using true differential buffers.

Intel® MAX® 10 High-Speed LVDS I/O User Guide

Trace widths are recommended to be 5 mil (0.127 mm) maximum, typical SerDes Applications commonly use 4 mil (0.1 mm) width traces for maximum lengths of up to 10 inches. Standard via sizes that allow escape from a 0.8-mm pitch device can be used (i.e., 8-mil holes, 18-mil pads).

SerDes Implementation Guidelines for Keystone Devices

The heterogeneous structure is faster, the binary-tree topology is the fastest. For this reason, 2:1 multiplier (MUX) and 1:2 demultipliers (DEMUX) are important elements for high-speed SerDes transceivers. In high-speed SerDes transceivers, there are usually tens of input ports of PISO and tens of output ports of SIPO.

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